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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,742	11/13/2003	Gerald Keith Bartley	ROC920030226US1	8903

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EXAMINER	
DOLE, TIMOTHY J	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/712,742	BARTLEY ET AL.	
	Examiner	Art Unit	
	Timothy J. Dole	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15* is/are rejected.

7)☒ Claim(s) *14,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinoshita et al. in view of Muntz.

Referring to claim 1, Hinoshita et al. discloses a method for implementing automated electronic package transmission line characteristic impedance verification comprising the steps of: generating a selected frequency coupled to a transmission line test structure (column 6, lines 30-33); measuring an input impedance with an open-circuit termination (column 1, lines 20-21) and a short-circuit termination (column 1, line 25) on said transmission line test structure; and using said input impedance measured value for said open-circuit termination and said short-circuit termination, calculating characteristic impedance (column 1, lines 27-43).

Hinoshita et al. does not disclose comparing said calculated characteristic impedance with threshold values for verifying acceptable electronic package transmission line characteristic impedance.

Muntz discloses characteristic impedance verification comprising the step of comparing said calculated characteristic impedance with threshold values for verifying

acceptable electronic package transmission line characteristic impedance (column 10, lines 23-27).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the comparison of Muntz into the method of Hinoshita et al. for the purpose of determining if fault conditions exist on the cable (column 10, lines 23-33).

Referring to claims 2 and 8, Hinoshita et al. discloses the method and apparatus as claimed, further including the steps of providing a pair of transmission line test structures respectively implemented at a package level with a open-circuit termination and a short-circuit termination (figs. 3D and 3E).

Referring to claims 3 and 9, Hinoshita et al. discloses the method and apparatus as claimed wherein the steps of measuring said input impedance with said open-circuit termination and said short-circuit termination for said transmission line test structure includes the steps of providing open-circuit impedance measuring circuitry (fig. 7 (32)) coupled to one of said pair of transmission line test structures; and providing short-circuit impedance measuring circuitry (fig. 7 (32)) coupled to another of said pair of transmission line test structures (column 9, lines 46-49).

Referring to claims 4 and 10, Hinoshita et al. discloses the method and apparatus as claimed, further including the steps of providing a single transmission line test structure (fig. 7) implemented at a package level and providing open-circuit and shod-circuit termination circuitry coupled to said single transmission line test structure (column 9, lines 59-60).

Referring to claim 5, Hinoshita et al. discloses the method as claimed wherein the steps of measuring said input impedance with said open-circuit termination and said short-circuit termination for said transmission line test structure includes the steps of sequentially providing an open-circuit termination and a short-circuit termination to said single transmission line test structure utilizing said open-circuit and short-circuit termination circuitry (column 9, lines 40-62).

Referring to claims 6 and 11, Hinoshita et al. discloses the method and apparatus as claimed except for the step of displaying a pass or fail result responsive to said compared values.

Muntz discloses the step of displaying a pass or fail result responsive to said compared values (column 3, lines 50-67). It should be noted that the computer end-stations of Muntz would include monitors to display all the data from the threshold comparison.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the display of Muntz into the method of Hinoshita et al. for the purpose of relaying important information to a user whereby making it possible to fix a fault that has been reported.

Referring to claims 7 and 15, Hinoshita et al. discloses an apparatus for implementing automated electronic package transmission line characteristic impedance verification comprising: a sinusoidal voltage source (fig. 7 (36)) coupled to a transmission line test structure (fig. 7) for generating a selected frequency (column 6, lines 30-33); impedance measuring circuitry (fig. 7 (32)) coupled to said transmission

line test structure for measuring an input impedance for an open-circuit termination and a short-circuit termination (column 1, lines 20-25); and characteristic impedance calculation circuitry (fig. 7 (38)) coupled to said impedance measuring circuitry for receiving said input impedance measured values with said open-circuit termination and said short-circuit termination for calculating characteristic impedance (column 1, lines 27-43).

Hinoshita et al. does not disclose logic circuitry coupled to said characteristic impedance calculation circuitry for comparing said calculated characteristic impedance with threshold values for verifying acceptable electronic package transmission line characteristic impedance; and said sinusoidal voltage source, said impedance measuring circuitry, said characteristic impedance calculation circuitry, and said logic circuitry being implemented by a single integrated circuit device.

Muntz discloses logic circuitry coupled to said characteristic impedance calculation circuitry for comparing said calculated characteristic impedance with threshold values for verifying acceptable electronic package transmission line characteristic impedance (column 10, lines 23-27); and said sinusoidal voltage source, said impedance measuring circuitry, said characteristic impedance calculation circuitry, and said logic circuitry being implemented by a single integrated circuit device. It should be noted that MPEP 2144.04 (V) (B) states that making features integral does not make the claims patentably distinct over the prior art of record unless there is a new or unexpected result. Since combining the limitations of claim 7 into a single integrated

circuit does not produce any unexpected results, making the parts integral does not make the claim patentably distinguishable over the prior art of record.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the logic circuitry of Muntz into the apparatus of Hinoshita et al. for the same purpose as given in claim 1, above.

Referring to claim 12, Hinoshita et al. discloses the apparatus as claimed wherein said characteristic impedance calculation circuitry calculates said characteristic impedance represented by: $Zo = (Zsc \times Zoc)^{1/2}$ where Zo represents said calculated characteristic impedance and Zoc and Zsc represent said input impedance measured values for said open-circuit termination and said short-circuit termination (column 1, lines 15-43).

Referring to claim 13, Hinoshita et al. discloses the apparatus as claimed except wherein said logic circuitry compares said calculated characteristic impedance with threshold values for verifying acceptable electronic package transmission line characteristic impedance represented by: $Z_1 < Zo < Z_2$ where Zo represents said calculated characteristic impedance and Z_1, Z_2 represent lower and upper threshold values for an electronic package characteristic impedance specification.

Muntz discloses said logic circuitry compares said calculated characteristic impedance with threshold values for verifying acceptable electronic package transmission line characteristic impedance represented by: $Z_1 < Zo < Z_2$ where Zo represents said calculated characteristic impedance and Z_1, Z_2 represent lower and upper threshold values for an electronic package characteristic impedance specification (column 10, lines 23-27).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the logic circuitry of Muntz into the apparatus of Hinoshita et al. for the same purpose as given in claim 1, above.

Allowable Subject Matter

3. Claims 14, 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to show the state of the art with respect to transmission line testing.

USPN 6,593,770 to Hernandez-Marti: This patent shows an apparatus for determining characteristic impedance using open circuit impedance and short circuit impedance.

USPN 5,636,147 to Tolmie et al.: This patent shows an apparatus for calculating characteristic impedance using open circuit impedance and short circuit impedance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Dole whose telephone number is (571) 272-2229. The examiner can normally be reached on Mon. thru Fri. from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571) 272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJD

V. Nguyen
4/15/2005

VINCENT Q. NGUYEN
PRIMARY EXAMINER